

Semiconductor Wafer With Grouped Integrated Circuit Die
Having Inter-Die Connections For Group Testing

ABSTRACT OF THE DISCLOSURE

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A method of forming a plurality of integrated circuit die on a semiconductor wafer (30). The method forms a first integrated circuit die (32_a) in a first area in a fixed position relative to the semiconductor wafer, by forming at least two devices (42_a) in the first area, the at least two devices selected from a group of active and passive devices, and by forming a first metal layer (62) comprising portions connecting to the at least two devices in the first area. The method also forms a second integrated circuit die (32_b) in a second area in a fixed position relative to the semiconductor wafer, the second area separated from the first area by a scribe area (34). The formation of the second integrated circuit die comprises the steps of forming at least two devices (42_b) in the second area, the at least two devices selected from a group of active and passive devices, and forming the first metal layer to further comprise portions connecting to the at least two devices in the second area. The method also forms the first metal layer to further comprise a portion electrically connecting a portion of the first metal layer in the first area to a portion of the first metal layer in the second area and thereby extending in the scribe area.